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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/960,152	09/21/2001	Robert E. Bickel	PD-200007	4264

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EXAMINER	
BADERMAN, SCOTT T	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/960,152	BICKEL, ROBERT E.	
	Examiner	Art Unit	
	Scott T Baderman	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-15 and 17-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-15 and 17-26* is/are allowed.

6)☒ Claim(s) *1-3 and 5-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 13-15 and 17-26 are allowed.

2. The following is an examiner's statement of reasons for allowance:

With respect to claims 13 and 25, the Examiner asserts that the novelty of the claims, when read as a whole, is "wherein bit selection is generated as a function of whether a first one of the plurality of processor group outputs is synchronous or asynchronous and whether the first one of the plurality of processor group outputs is always valid or valid based on a state of a second one of the plurality of outputs.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 and 6-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fuchs et al. (6,141,770) in view of Williams (6,247,143).

As in claim 1, Fuchs discloses a fault tolerant processing circuit that comprises at least three processor groupings each of said at least three processor groupings having a plurality of processor grouping inputs and a plurality of processor grouping outputs (Figures 1 and 3), a processor system clock coupled to the fault tolerant processing circuit (Abstract), a synchronizing circuit comprising a plurality of output synchronizers, each output synchronizer in operative communication with a corresponding respective processor grouping for synchronizing the output of each processor grouping (Abstract, column 7: lines 1-8, column 10: lines 8-11), a logic circuit in operative communication with said synchronizing circuit (Figures 3 and 6), said logic circuit comprising a fault detection circuit and a fault mask circuit (Figure 3, column 7: lines 24-43, column 9: lines 4-6, column 10: line 28 – column 11: line 14), said logic circuit adapted to compare said plurality of processor group outputs to detect errors in any one of said plurality of processor group outputs through selecting bits (i.e., the output data that is compared) from the processor group outputs (Figure 3, column 10: line 28 - column 11: line 14), and a control logic circuit for resetting each of said at least three processor groups when none of said at least three processor groups is in a majority of said processor groups (Figure 6, Abstract, column 13: lines 1-42), wherein said fault mask circuit is adapted to mask the output of a respective processor grouping associated with a detected error and signal a detected error (column 9: lines

4-6). However, Fuchs does not clearly disclose wherein the bit selection is generated as a function of whether a first one of the plurality of processor group outputs is synchronous or asynchronous. Williams discloses a fault tolerant system that selects and compares the outputs of processor units, wherein the processor units can be synchronous or asynchronous with one another (Figure 3, Abstract, column 2: lines 49-67, column 3: line 64 – column 4: line 25).

It would have been obvious to a person skilled in the art at the time the invention was made to include selecting and comparing output data (bits) from a plurality of processor groups as a function of whether a first one of the plurality of processor group outputs is synchronous or asynchronous into the system taught by Fuchs above. This would have been obvious because Williams teaches of a system similar to Fuchs, wherein synchronous processor groups can be monitored by comparing their outputs (column 1: lines 10-22). However, Williams, also teaches that other processing groups do not behave in the same way (i.e., they are not synchronous with one another) (column 1: lines 23-33). Due to these processing groups not being synchronous with one another, Williams provides a system for a reliable efficient handling of I/O operations in a multiprocessor system wherein the processors are asynchronous with one another (column 1: lines 39-43). A person skilled in the art would have understood the similarities between Fuchs and Williams, and further, would have also understood the fact that some processors will operate asynchronous with one another through the teaching of Williams (see above). Further, a person skilled in the art would have been led to include the teachings of Williams into the system taught by Fuchs in order to overcome the scenario wherein the processor groups are asynchronous with one another being that Williams clearly teaches that this is common amongst multiple processors (column 1: lines 10-43).

As in claim 2, Fuchs discloses wherein said synchronizing circuit further comprises continuously active synchronization signals (i.e., every clock cycle) (Abstract, column 7: lines 1-8).

As in claim 3, Fuchs discloses wherein said synchronizing circuit further comprises periodically active synchronization signals (i.e., every clock cycle is considered periodic) (Abstract, column 7: lines 1-8).

As in clam 6, Fuchs discloses wherein an expected rate of transient faults is tuned by a latent fault scrubbing rate (Figure 4, column 11: lines 35-55).

As in claim 7, Fuchs discloses wherein each of said at least three processor groupings comprises a central processing unit (CPU), having an operating step executed during a clock cycle and operating synchronously with each other CPU, each operating step of each CPU being accomplished in parallel and substantially simultaneously with each of the other at least three CPUs each clock cycle (Figure 3, column 7: lines 1-8), each of said at least three CPUs having a plurality of CPU inputs and a plurality of CPU outputs (Figure 3), and a respective support logic device coupled to said plurality of CPU inputs and said plurality of CPU outputs and having a plurality of support logic device inputs and outputs coupled to said respective CPU (i.e., this is interpreted as the bus interface and system bus components connected to the system bus) (Figure

3).

As in claim 8, Fuchs discloses wherein said logic circuit resets each of said at least three processor groups upon detected a fault and, in response, each of said at least three processor groups restart at a hardware defined operating step (state) (Figure 6, column 11: lines 1-4, column 16: lines 2-4).

As in claim 9, Fuchs discloses wherein said logic circuit interrupts said at least three processor groups when one of said processor groups has a fault, whereby each of said at least three processor groups without detected faults store state information and said logic circuit resets each of said at least three processor groups after said state information is stored to restart said at least three processor groups at a state defined operating step (Figure 6, column 13: lines 1-31, column 14: lines 53-54, column 15: line 4 – column 16: line 6).

As in claim 10, Fuchs discloses wherein said logic circuit interrupts said at least three processor groups when a minority of said processor groups has a fault, and wherein each of said at least three processor groups without an error stores state information and said logic circuit resets each of said at least three processor groups after said state information is stored to restart said at least three processor groups at a state defined operating step (Figure 6, column 13: lines 1-31, column 14: lines 53-54, column 15: line 4 – column 16: line 6).

As in claim 11, Fuchs discloses wherein said logic circuit includes fault control and status registers for storing said state information (Figures 6 and 8, column 15: lines 44-56).

As in claim 12, Fuchs discloses wherein each of said at least three support logic devices includes a memory system (Figure 3).

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fuchs et al. and Williams, and in further view of Golshan (6,671,841).

As in claim 5, Fuchs and Williams discloses the system above. However, neither clearly disclose wherein said synchronizing circuit further comprises logic operative to synchronize a JTAG TCLK with said processor system clock. Golshan discloses that the JTAG standard requires a clock that operates at a different frequency of the internal clock, and thus need to be synchronized with the internal clock to avoid skew problems (Figure 4, column 5: lines 35-50, column 6: lines 27-38).

It would have been obvious to a person skilled in the art at the time the invention was made to include a logic operative to synchronize a JTAG TCLK with said processor system clock into the system taught by Fuchs and Williams above. This would have been obvious because Fuchs is not limited form including JTAG circuitry, which is very popular in today's computer processors. A person skilled in the art would have understood that is highly likely that the processors taught by Fuchs does include JTAG circuitry, and if so, would need to make sure

that the JTAG signals are synchronized with the internal clock to avoid skew problems, as was taught by Golshan above.

Response to Arguments

6. Applicant's arguments with respect to claims 1-3 and 5-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott T Baderman whose telephone number is (571) 272-3644. The examiner can normally be reached on Monday-Friday, 6:45 AM-4:15 PM, first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Scott T Baderman
Primary Examiner
Art Unit 2113

STB